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## AMENDMENTS TO CLAIMS

- Please amend pending claims 1 and 8 as indicated below. A complete listing of all claims and their status in the application are as follows:
  - 1. (currently amended) An integrated circuit interconnect comprising: a wide top metal line;
  - a wide bottom metal line;
  - a dielectric layer disposed between the wide top and wide bottom metal lines;
  - a plurality of vias in the dielectric layer and connecting the wide top and wide bottom metal lines including:
    - a first via having a width, and
    - a second via having a width and spaced more than two widths away and less than four widths away from the first via with no intervening vias.
  - 2. (original) The integrated circuit as claimed in claim 1 wherein: the second via is spaced from the first via in a direction perpendicular to the length of the wide top metal line; and including:
    - a third via having a width and spaced more than two widths and less than four widths from the first via in a direction parallel to the length of the wide top metal line.
  - 3. (original) The integrated circuit as claimed in claim 1 wherein: the second via is spaced from the first via in a direction parallel to the length of the wide top metal line; and including:
    - a third via having a width and spaced more than two widths and less than four widths from the first via in a direction perpendicular to the wide top metal line.
  - (original) The integrated circuit as claimed in claim 1 wherein:
    the dielectric layer has an opening provided therein equidistant from the first and second vias.
  - 5. (original) The integrated circuit as claimed in claim 4 wherein: the opening which has a width equal to the width of the first via.

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- 6. (original) The integrated circuit as claimed in claim 4 wherein: the opening has a length greater than twice the width thereof.
- 7. (original) The integrated circuit as claimed in claim 4 wherein: the opening has a length and the length extends perpendicular to the length of the wide top metal line.
- 8. (currently amended) An integrated circuit interconnect comprising: a wide top metal line;
- a wide bottom metal line;
- a dielectric layer disposed between the wide top and wide bottom metal lines; and
- a via-sea in the dielectric layer and connecting the wide top and wide bottom metal lines including:
  - a first column of vias having a width, and
  - a second column of vias having a width and spaced more than two widths away and less than four widths away from the first column of vias with no intervening vias.
- 9. (original) The integrated circuit as claimed in claim 8 wherein:
- the second column of vias is spaced from the first column of vias in a direction perpendicular to the length of the wide top metal line; and including:
  - a first row of vias including a via in the first column of vias having a width and spaced more than two widths and less than four widths from the first column of vias in a direction parallel to the wide top metal line.
- 10. (original) The integrated circuit as claimed in claim 8 wherein:
- the second column of vias is spaced from the first column of vias in a direction parallel to the length of the wide top metal line; and including:
  - a first row of vias including a via in the first column of vias having a width and spaced more than two widths and less than four widths from the first column of vias in a direction perpendicular to the wide top metal line.

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- 11. (original) The integrated circuit as claimed in claim 8 wherein: the dielectric layer has an opening provided therein equidistant from the first column of vias and the second column of vias.
- 12. (original) The integrated circuit as claimed in claim 11 wherein: the opening has a width equal to the width of the first column of vias.
- 13. (original) The integrated circuit as claimed in claim 11 wherein: the opening has a length greater than twice the width thereof.
- 14. (original) The integrated circuit as claimed in claim 11 wherein: the opening has a length and extends perpendicular to the length of the wide top metal line.